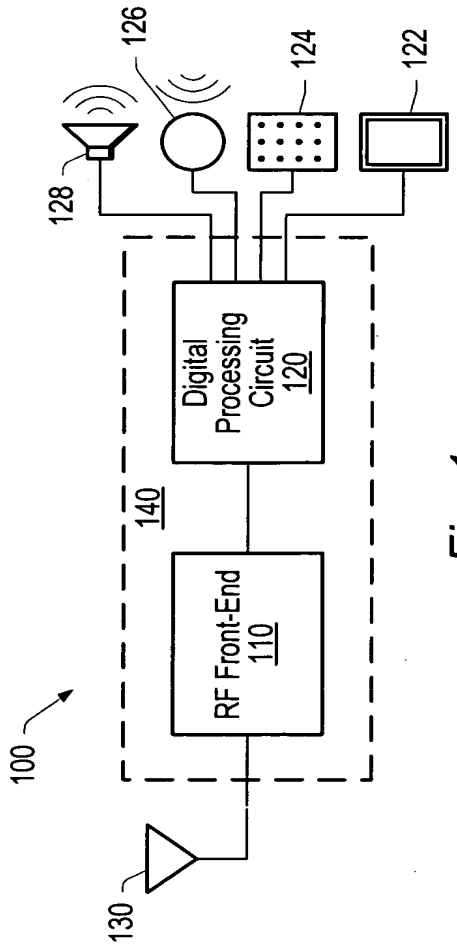
100
130
140
RF Front-End
110
Digital
Processing
Circuit
120
128
126
124
122

Fig. 1

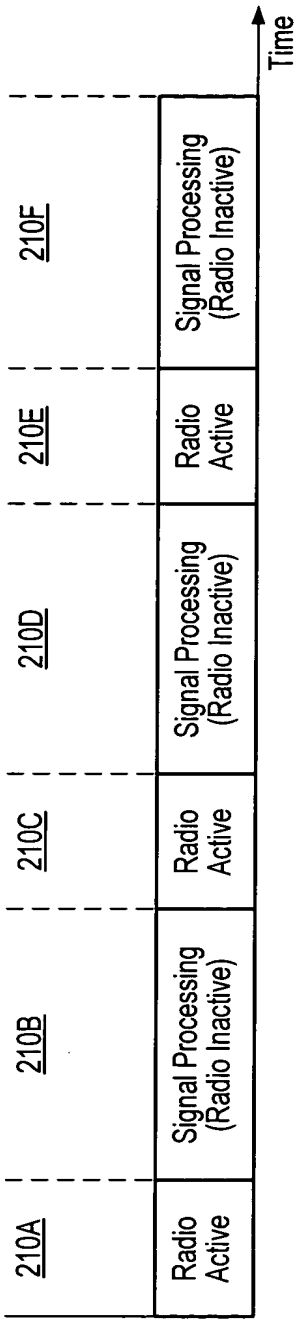
210A
210B
210C
210D
210E
210F
Radio
Active
Signal Processing
(Radio Inactive)
Radio
Active
Signal Processing
(Radio Inactive)
Radio
Active
Signal Processing
(Radio Inactive)
Time

Fig. 2

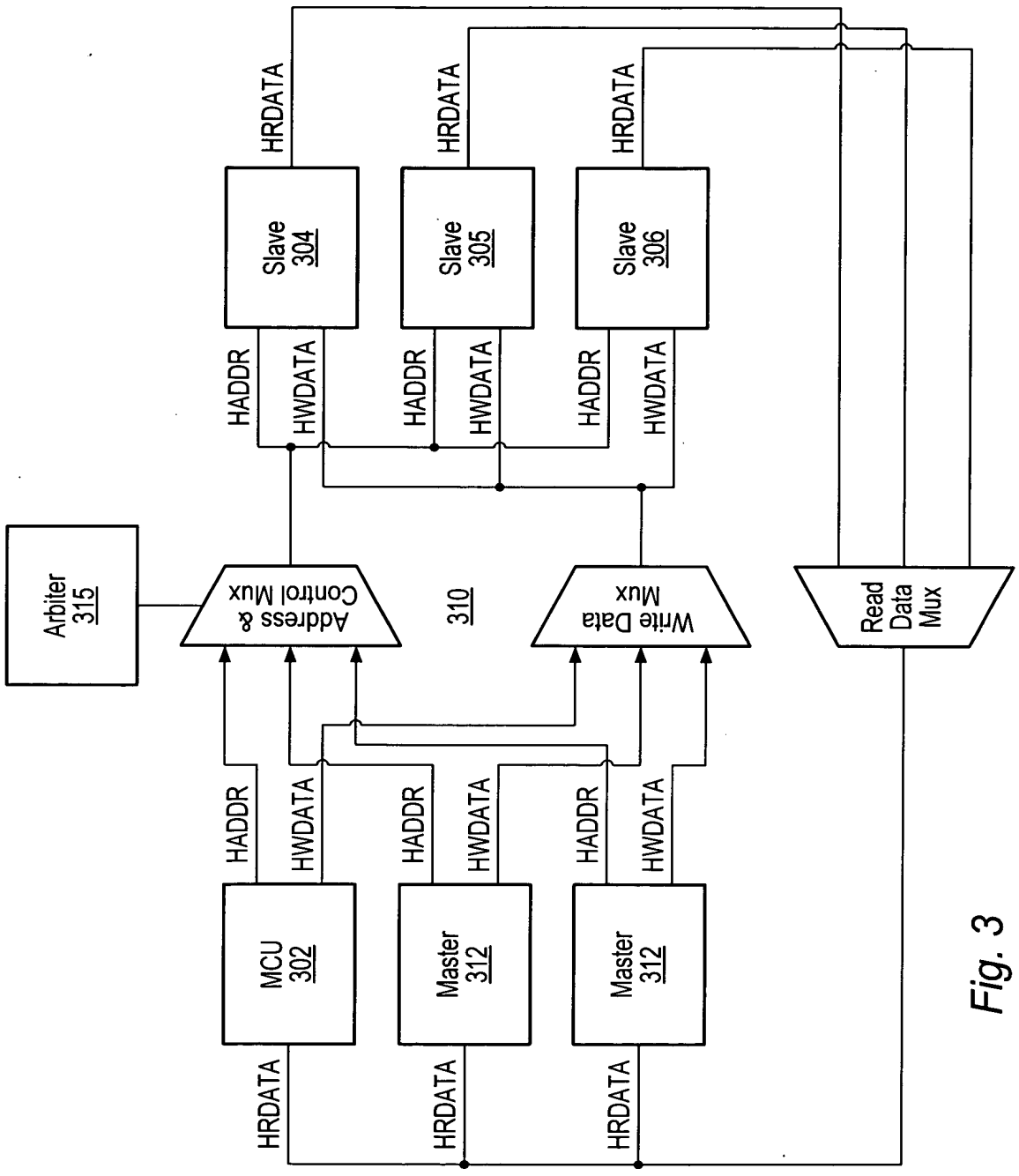
Arbiter 315
Address & Control Mux
310
Write Data Mux
Read Data Mux
MCU 302
Master 312
Master 312
Slave 304
Slave 305
Slave 306
HADDR
HWDATA
HRDATA

Fig. 3

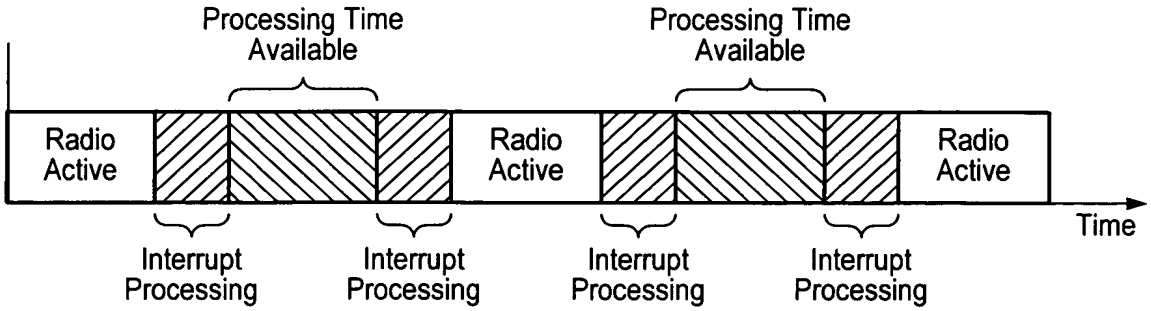
Processing Time Available
Processing Time Available
Radio Active
Radio Active
Radio Active
Time
Interrupt Processing
Interrupt Processing
Interrupt Processing
Interrupt Processing

Fig. 4A

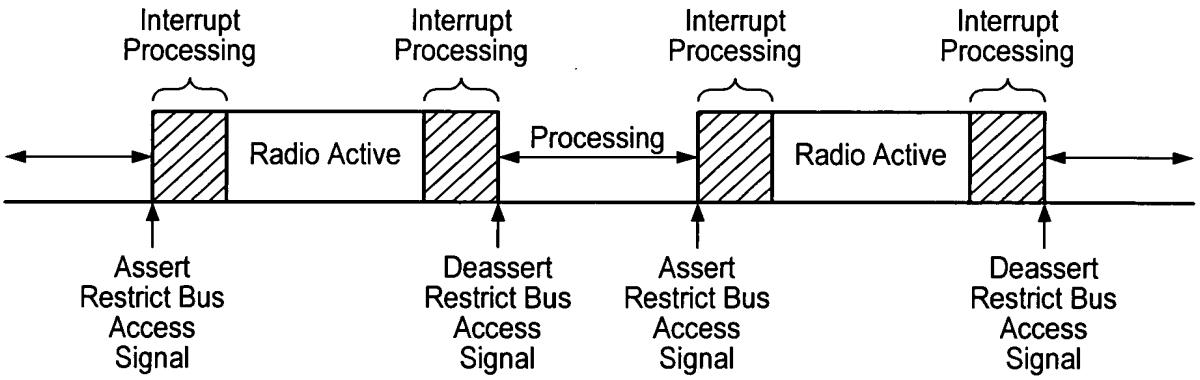
Interrupt Processing
Interrupt Processing
Interrupt Processing
Interrupt Processing
Radio Active
Processing
Radio Active
Assert Restrict Bus Access Signal
Deassert Restrict Bus Access Signal
Assert Restrict Bus Access Signal
Deassert Restrict Bus Access Signal

Fig. 4B

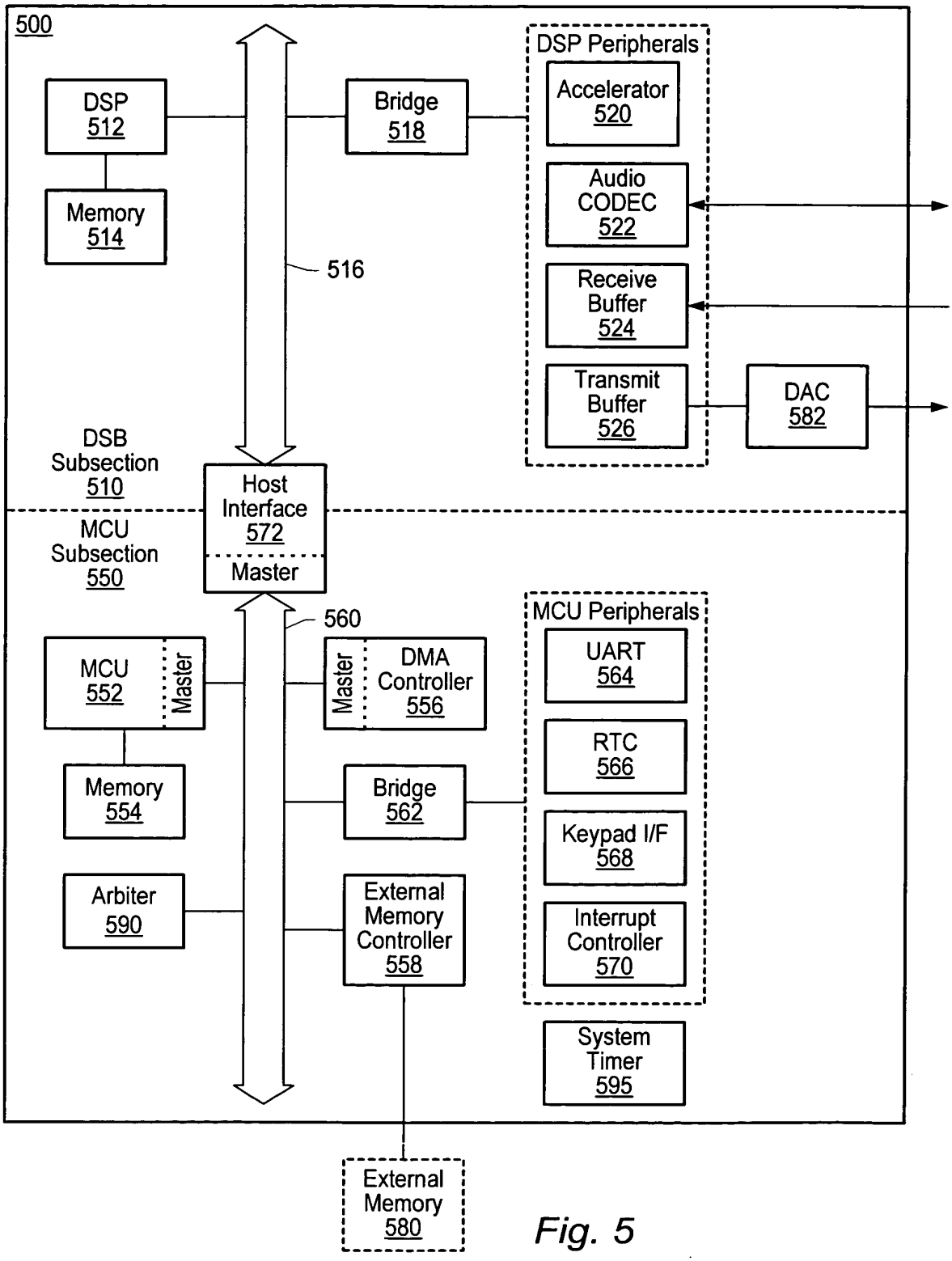
500
DSP
512
Memory
514
Bridge
518
516
DSP Peripherals
Accelerator
520
Audio
CODEC
522
Receive
Buffer
524
Transmit
Buffer
526
DAC
582
DSB
Subsection
510
MCU
Subsection
550
Host
Interface
572
Master
560
MCU
552
Master
Memory
554
Arbiter
590
Master
DMA
Controller
556
Bridge
562
External
Memory
Controller
558
MCU Peripherals
UART
564
RTC
566
Keypad I/F
568
Interrupt
Controller
570
System
Timer
595
External
Memory
580

Fig. 5

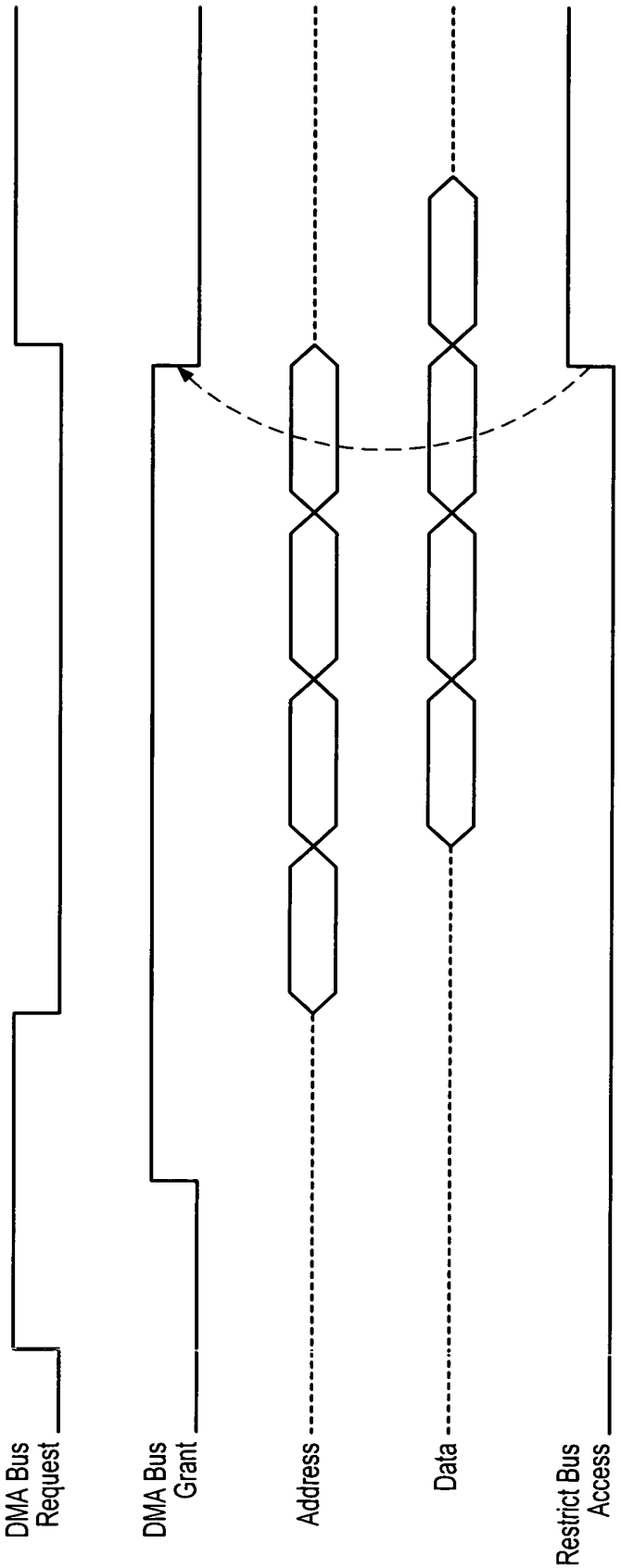
DMA Bus Request
DMA Bus Grant
Address
Data
Restrict Bus Access

Fig. 6

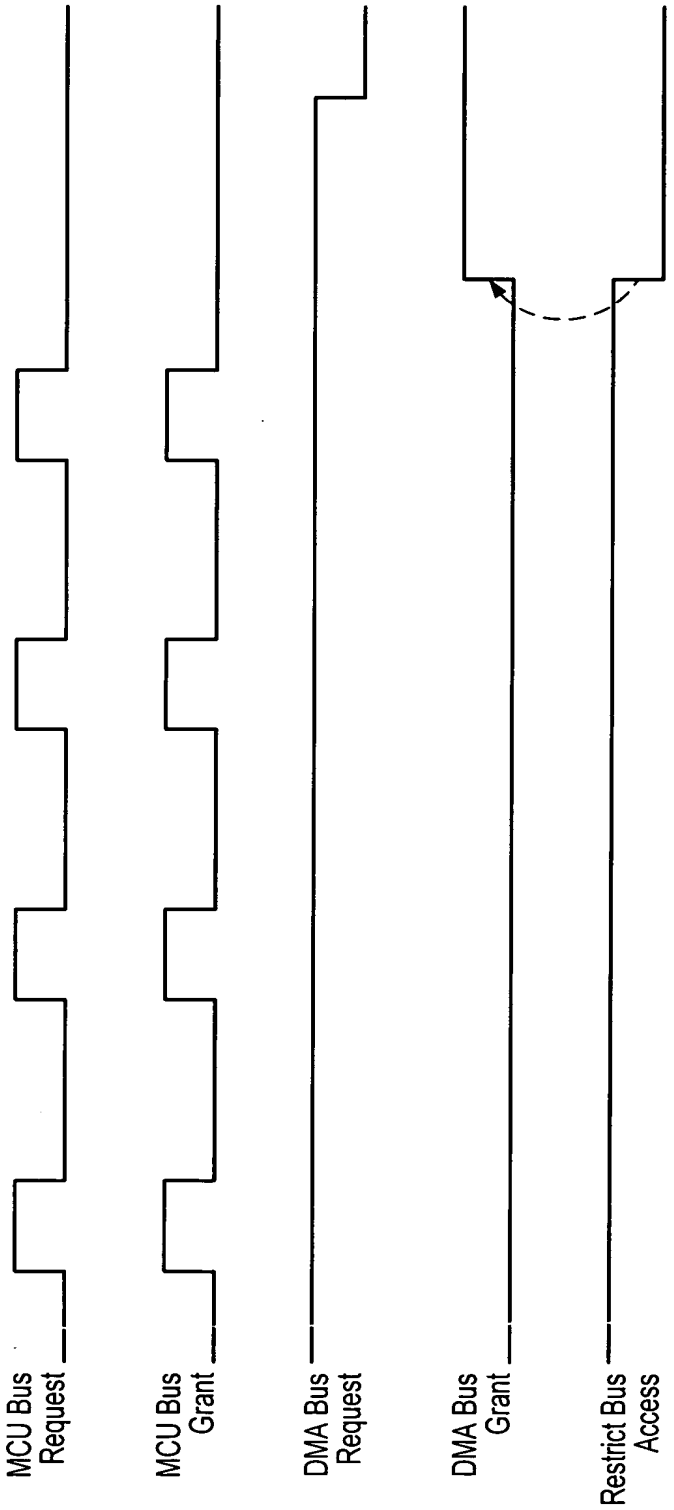
MCU Bus Request
MCU Bus Grant
DMA Bus Request
DMA Bus Grant
Restrict Bus Access

Fig. 7